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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,468	08/26/2003	Osamu Abe	2002-249352US	2305

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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,468	ABE, OSAMU	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, and 5-6* is/are rejected.

7)☒ Claim(s) *4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08262003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: P01, P02, N01, and C01 shown in Fig. 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "R1" has been used to designate both a resistor coupled between R2 and D1 in Figs. 1, 2, and 10, as well as a resistor coupled between N2 and D2 in Fig. 8; reference character "R2" has been used to designate both a resistor coupled between VOUT and D2 in Figs. 1-2, as another resistor that is coupled between VOUT and R1 in Figs. 1, 2, and 10, and as a resistor coupled between VOUT and D3 in Fig. 8; reference characters "P1" and "P2" are

shown configured as a current mirror in Fig. 8 with P2 as the diode connected transistor, wherein the P1/P2 current mirror in Fig. 10 has P1 as the diode connected transistor; and reference characters "N1" and "N2" are shown in Fig 8 configured as a current mirror, but as a pair of differential input transistors in Fig. 10. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance. Also, if the drawings are changed to provide more consistent labeling, without redundancy, within the figures, corresponding changes will need to be made to each figure's description.

Specification

The applicant is reminded of the proper language for an abstract of the disclosure. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc. In this case, the "relating to the present invention" phrase on lines 3-4 and 14-15 are understood because the abstract should be related to (e.g. describing) the disclosed invention. It is suggested "In a band gap circuit relating to the present invention that" on lines 3-4 be changed to --A band gap circuit--; and the term --wherein-- be added after "amplifier," on line 4. Also, the phrase "relating to the

present invention" on lines 14-15 should be deleted to remove the implied "present invention" phrasing.

The abstract of the disclosure is objected to because it is not clear how the singular "a resistor R2" actually relates to the two resistors identified with "R2" that are shown within the applicant's Figs. 1, 2, and 10. For example, does the capacitive component of the "resistor" relate to the combined components of both resistors, or to only one of them? If it relates to only one resistor "R2", are both resistors of equal size? Correction and/or clarification are required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: Page 15, line 20 "register" should be --resistor--. Although the description on page 16, lines 12-15 does correspond to the connections of the one resistor "R2" shown to the outermost right side of Fig. 1, it is believed lines 12-15 should be referring to the other resistor R2 (shown to the left of the right "R2") which has one end coupled to the gate of P1 and D2, and the other end connected to VOUT. However, as presently written, the description on lines 12-15 corresponds to the connections of resistor R2 already described on lines 6-9. [Note: This confusion relates to the labeling of two separate resistors as "R2" shown in the figures.] Page 22, lines 10-12 should be clarified with respect to Fig. 1 and "transistors 15." For example, only Fig. 2 shows transistor 15, and it is shown only as a single transistor. Related to the two resistors identified as "R2" within the figures, are the descriptions on pages 38-41 referring to identical resistors "R2", or to only one specific "R2" resistor? Page 36, line 16 "direct-current power supply" should be

--constant current source-- to be consistent with the descriptions on lines 9-10 and 13 of the same page. Page 37, line 4 "Vb2" should be --Vb1-- to correspond to the connection shown in Fig. 2. Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Mottola et al. (Mottola). Fig. 3 shows band gap circuit 200 for generating output voltage VBG at circuit output terminal 203, wherein band gap circuit 200 is connected to power supply voltage Vcc and reference potential 104 (e.g. ground). Band gap circuit 200 comprises differential amplifier Q2-Q6,Q8,Q9, having inverting/noninverting input terminals (e.g. bases of Q2 and Q3), and an output terminal (e.g. common connection between Q6 and Q9); first circuit R1,R2,Q1 for causing a potential difference to the input terminals in response to fluctuation of voltage VBG on circuit output terminal 203; and switching element Q7 connected between circuit output terminal 203 and reference potential 104, as well as being directly connected to the output terminal of the differential amplifier. Since Mottola discloses that switching element Q7 sinks additional bootstrap current IBS to ensure regulation of voltage VBG (e.g. see column 7, lines 1-6), one of ordinary skill in the art would understand switching element Q7 causes excess current of circuit

output terminal 203to flow in (to) reference potential 104 in response to fluctuation of potential at the output terminal of differential amplifier Q2-Q6,Q8,Q9, thus anticipating claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottola et al. as applied to claim 1 above, and further in view of Oda. As previously described, Fig. 3 of Mottola shows band gap circuit 200 comprising a differential amplifier, first circuit, and switching element to read on the limitations recited within claim 1. However, the reference does not clearly show or disclose first/second elements having resistive/capacitive components, respectively for removing power supply noise. Fig. 1 of Oda shows the use of first element R1, C1 with resistive component R1, and second element C2 with capacitive component C2, coupled to output Vo of reference voltage generating source 1, as a means for removing noise related to power source VDD (e.g. see column 1, lines 29-33). Therefore, it would have been obvious to one of ordinary skill in the art to apply the teaching, and/or first/second elements, of Oda to the band gap circuit (one known type of reference voltage generating source) of Mottola. For example, first element R1,C1 and second element C2 of Oda could be coupled to circuit output terminal 203 of Mottola's band gap circuit, thus rendering claim 2 obvious. The elements would be one known means for removing (high-frequency) noise with respect to power supply voltage Vcc. Although first element R1,C1 of Oda does have resistive component R1, the Oda reference

does not clearly show or disclose the first element with a transistor. However, it would have been obvious to one of ordinary skill in the art to use a transistor as resistive element R1. Therefore, when this first element/transistor is coupled to Mottola's output terminal, along with the associated second element C2, claim 3 is also rendered obvious. The use of a transistor as a resistive device allows the user of the overall system a means for adjusting the resistive component of the device by varying a bias voltage applied to the control electrode of the transistor. In this case, since R1,C1,C2 of Oda functions as a low pass filter (e.g. see column 1, lines 29-31), one of ordinary skill in the art would know that an adjustment to the resistive component will affect what frequencies the LPF will pass/remove. Therefore, the transistor will allow the user to adjust the noise removal, depending on the desired results.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mottola et al. (Mottola) in view of Oda. Fig. 3 of Mottola shows band gap circuit 200 for generating output voltage VBG at circuit output terminal 203, wherein band gap circuit 200 is connected to power supply voltage Vcc and reference potential 104 (e.g. ground). Band gap circuit 200 comprises differential amplifier Q2-Q6,Q8,Q9, having inverting/noninverting input terminals (e.g. bases of Q2 and Q3), and an output terminal (e.g. common connection between Q6 and Q9); first circuit R1,R2,Q1 for causing a potential difference to the input terminals in response to fluctuation of voltage VBG on circuit output terminal 203; and switching element Q7 connected between circuit output terminal 203 and reference potential 104, as well as being connected to the output terminal of the differential amplifier. Since Mottola discloses that switching element Q7 sinks additional bootstrap current IBS to ensure regulation of voltage VBG (e.g. see column 7, lines 1-6), one of ordinary skill in the art would understand switching element Q7 causes excess current

of circuit output terminal 203 to flow in (to) reference potential 104 in response to fluctuation of potential at the output terminal of differential amplifier Q2-Q6,Q8,Q9. However, the Mottola reference does not clearly show or disclose first/second elements having resistive/capacitive components, respectively for removing power supply noise. Fig. 1 of Oda shows the use of first element R1,C1 with resistive component R1, and second element C2 with capacitive component C2, coupled to output Vo of reference voltage generating source 1, as a means for removing noise related to power source VDD (e.g. see column 1, lines 29-33). Therefore, it would have been obvious to one of ordinary skill in the art to apply the teaching , and/or first/second elements, of Oda to the band gap circuit (one known type of reference voltage generating source) of Mottola. For example, first element R1,C1 and second element C2 of Oda could be coupled to output VBG of Mottola's band gap circuit, wherein first element R1,C1 could be connected between power supply voltage Vcc and circuit output terminal 203, and second element C2 could be coupled to first element R1,C1 (i.e. at circuit output terminal 203), thus rendering claim 5 obvious. The elements would be one known means for removing any (high-frequency) noise with respect to power supply voltage Vcc. Although first element R1,C1 of Oda does have resistive component R1, the Oda reference does not clearly show or disclose the first element with a transistor. However, it would have been obvious to one of ordinary skill in the art to use a transistor as resistive element R1. Therefore, when this first element/transistor is coupled to Mottola's output terminal, along with the associated second element C2, claim 6 is also rendered obvious for the same reasoning as described with respect to claim 3 earlier.

No claim is allowable.

Allowable Subject Matter

However, claims 4 and 7 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure the second element, with a capacitive component, is an "ion implantation resistor" as recited within both claims 4 and 7.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. McNeill et al. and Moreland et al. are of special interest. Although neither of these two references was used in any formal rejections described above, both show band gap circuits comprising a differential amplifier; a first circuit for causing a potential difference; and one type of switching element. For example, see McNeill et al. (Fig. 1: 112; M1-M2,R1, Q1-Q2; and M3,M4) and Moreland et al. (Fig. 2: Q6-Q7,Q9-Q11; 31; and Q8,Q12). It is also noted that Moreland et al. discloses Q8 sinks current from output node N3 (e.g. see column 4, lines 22-24). Fig. 1 of Kim et al. shows an example of a band gap circuit corresponding to the applicant's own Prior Art Fig. 10. Therefore, these references should be reviewed and considered carefully.

The prior art references cited on the IDS submitted on Aug 26, 2003 were reviewed and considered. Neither of the references clearly shows or discloses the switching element of a band gap circuit for causing excess current of the circuit output terminal to flow in (to) the reference potential.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

13 August 2004

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